Docket Number 0041153 Mailing Number 162933

Mailing Date May, 11, 2004

NOTICE OF REASONS OF REJECTION

Application Number	Pat Appln 2001-031320
Date of Draft	April 30, 2004
Patent Office Examiner	Hidetada MATUSHIMA
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Attorney of Applicant	Keishirou TAKAHASHI
Applied Article	Article 29, 1st paragraph
	Article 29, 2nd paragraph
	Article 37

This application should be rejected by the following reasons. When the applicant has opinion thereto, please submit Argument within 60 days from the date of mailing.

REASONS

<Reason 1>

The application does not satisfy the requirements stipulated in the Japanese Patent Law, Article 37 in the following points.

Remarks

Memorandum

The issue common with the invention described in claims 1 - 4 and

the invention described in claims 5 - 10 is "to provide a semiconductor device and its manufacture method capable of storing two-bit information in one memory cell and being driven at a low voltage". However, this issue was solved before the filing of this application (e.g., refer to Y. Hayashi et al., Twin MONOS Cell with Dual Control Gates, 2000 Symposium on VLSI Technology Digest of Technical Papers, PP. 122-123, and Korean Patent Laid-open Publication Nc. 2000-0076792) and is not an issue still not solved when this application was submitted so that both the inventions do not satisfy the Japanese Patent Law, Article 37, first paragraph.

The configuration that "a conductive member is disposed on a lamination film including a carrier trap layer and a gate voltage is directly applied to the conductive member", which is the invention specifying item corresponding to the issue to be solved and common with both the inventions, is disclosed in the above-mentioned documents, so that there exists no substantial part of a novel invention specifying item corresponding to the issue to be solved and both the inventions do not satisfy the Japanese Patent Law, Article 37, third, fourth and fifth paragraphs.

Since this application violates the stipulations of the Japanese Patent Law, Article 37, the inventions regarding the claims other than claims 1 - 4 were not examined with respect to the requirements such as novelty and inventive step.

As to the claims other than claims 1 - 4, refer to the documents and etc described in Records of Search Results of Prior Art Technical Documents.

<Reason 2>

The invention relating to the following claim of this application is the invention described in the below-mentioned publications distributed in Japan or in foreign countries prior to the filling of this application or the invention made available to general public via electronic communication lines. Therefore, this application cannot be granted a patent under the stipulation of item 3,

paragraph 1 of Article 29 of the Japanese Patent Law.

<Reason 3>

The invention relating to the following claim of this application could be easily made by those skilled in the art before the filling of this application, based on the invention described in the below-mentioned publication distributed in Japan or foreign countries prior to the filing of this application or on the invention made available to general public via electronic communication lines. Therefore, this application cannot be granted a patent under the stipulation of paragraph 2 of Article 29 of the Japanese Patent Law.

Remarks

(refer to a list of cited documents and others)

Claim 1

Reasons 2, 3

Cited Document 1

Memorandum

Refer particularly to Fig. 1 and its description of the Cited Document 1.

The Cited Document 1 describes that a trap film made of an ONO film and side walls made of polysilicon are formed on both sides of a gate electrode, and also describes that the gate electrode and the side walls made of polysilicon are electrically connected.

Claim 2

Reason 3

Cited Documents 1, 2, 3

Memorandum

A memory array structure of a virtual ground type is well-known technologies when the application was submitted (e.g., refer to Figs. 1 to 6 and their description of the Cited Document 2 and Fig. 1 and its description of the Cited Document 3).

The rejection reasons are not found at this time for the invention of claims 3 and 4 other than the claims referenced in this Notice of Reasons of Rejection. When the rejection reason is newly found, Notice of Reasons of Rejection is notified.

List of Cited Documents and Others

1. Korean Patent Laid-open Publication No. 2000-0076792
2. Japanese Patent Laid-open Publication No. HEI-05-326893
3. Boaz Eitan et al., NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell, IEEE ELECTRON DEVICE LETTERS, November. 2000, VOL. 21, NO. 11, PP. 543-545

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Records of Search Results of Prior Art Technical Documents

Searched Fields

IPC Version 7 H01L29/792

H01L27/115

H01L21/8247

Prior Art Technical Publications

Japanese Patent Publication No. 2003-508920

Japanese Patent Laid-open Publication No. 2001-118943

Japanese Patent Laid-open Publication No. 2001-230332

Japanese Patent Publication No. 2001-512290

Japanese Patent Laid-open Publication No. 2000-004014

The records of these prior art technical publication search results will not form reasons of rejection.